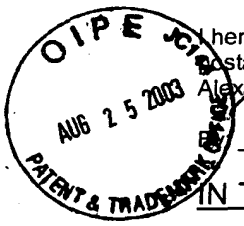
Docket No.: P2000,0361



I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

By: _____ Date: August 21, 2003

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Wolfgang Dickenscheid et al.
Applic. No.	:	10/609,464
Filed	:	June 27, 2003
Title	:	Method for Characterizing and Simulating a Chemical Mechanical Polishing Process

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner for Patents

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

J. Tony Pan et al.: "Planarization and Integration of Shallow Trench Isolation", *1998 Proceedings of the Fifteenth International VLSI Multilevel Interconnection Conference (VMIC), Santa Clara, CA, June 16-18, 1998, pp. 467-472*;

George Y. Liu et al.: "Chip-Level CMP Modeling and Smart Dummy for HDP and Conformal CVD Films", *1999 Proceedings of the Fourth International Chemical-Mechanical Planarization for ULSI Multilevel Interconnection Conference (CMP-MIC), Santa Clara, CA, February 11-12, 1999, pp. 120-127*;

Valeriy Sukharev: "Addressing the pattern density effects in deposition, etch and CMP by means of simulations", *2001 Proceedings of the Sixth International Chemical-Mechanical Planarization for ULSI Multilevel Interconnection Conference (CMP-MIC), Santa Clara, CA, March 7-9, 2001, pp. 403-413*;

Carsten Schmitz et al.: "CMPSIM – Ein Simulator für den Planarisierungsprozess auf Layout Ebene" [CMPSIM – a simulator for the planarization process on the layout level], *internal memo, Infineon Technologies AG, München, November 26, 1999, pp. 1-17.*

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and/or publications, it is because no existing translation is readily available to the applicant.

Respectfully submitted,

Mark P. Weichselbaum
Reg. No. 43,248

For Applicants

Date: August 21, 2003

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PATENT & TRADEMARK OFFICE

FORM PTO-1449 (SUBSTITUTE) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))	Attorney Docket No.: P2000,0361 Applic. No. 10/609,464 Applicant: Wolfgang Dickenscheid et al. Filing Date: June 27, 2003 Group Art Unit:

U.S. PATENT DOCUMENTS

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A						
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	I						

FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	TRANSL. NO
	J							
	K							
	L							
	M							
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

	O	J. Tony Pan et al.: "Planarization and Integration of Shallow Trench Isolation", *1998 Proceedings of the Fifteenth International VLSI Multilevel Interconnection Conference (VMIC), Santa Clara, CA, June 16-18, 1998, pp. 467-472*
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EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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INFORMATION DISCLOSURE
STATEMENT BY APPLICANT
(37 CFR 1.98(b))

Attorney Docket No.:	Applic. No.
P2000,0361	10/609,464

Applicant: Wolfgang Dickenscheid et al.

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